REMARKS

The rejections are improper because they continue to refer to a "Sin" reference that appears to be a reference cited in prior Office Action's of record but is no longer relied upon in the instant Office Action. The Office Action's allegations of motivation for modifying the newly-cited '944 reference are similarly improper because they refer to a modification of the "Sin" reference. Accordingly, none of the rejections can stand. Should any rejections be maintained, Applicant requests clarification (in the form of a non-final communication) and an opportunity to respond thereto. Notwithstanding the above, Applicant has reviewed the newly-cited '944 reference and submits that the reference fails to disclose the claimed invention as asserted, and generally fails to correspond to (or recognize the benefits of) the claimed invention as a whole. The following addresses the rejections in greater detail.

The Office Action dated March 4, 2009, indicated that claims 1-7, 9-17, 32-36, 38-39 and 43 stand rejected under 35 U.S.C. § 102(b) over Mizutani et al. (U.S. 5,616,944); claims 30, 31 and 37 stand rejected under 35 U.S.C. § 102(b) over Akimoto et al. (U.S. Pub. 2002/0117689); and claims 8 and 18-29 stand rejected under 35 U.S.C. § 103(a) over the '944 reference as applied to claim 1, and further in view of Baba (US 5,589,696). Applicant respectfully traverses each of the rejections, and in the discussion set forth below, does not acquiesce to any rejection or averment in this Office Action unless Applicant expressly indicates otherwise.

The § 102 rejections are improper because the '944 reference, upon which all rejections rely, fails to disclose various limitations as asserted, including those directed to controlling the electric field distribution in an intermediate region of a semiconductor device for rapid switching. While the cited portions of the '944 reference discuss a diode structure having a gate-controlled electric field distribution, the gate is centered upon an intrinsic region, the operation of the gate evenly affects the potential of the impurity region 16 "as a whole" (rather than closer to one or another junction as claimed; *see* column 5:43-44), and implementation of the gate generally fails to comprehend or disclose various aspects of the claimed invention. For example, the '944 reference (alone or in combination) fails to disclose limitations directed to structure and operation for rapid transitioning between ON and OFF states, including limitations directed to the use of a gate that is offset to affect the electric field at one of the junctions (*i.e.*, at one of the junctions in a P-I-N structure) as shown, for example, in FIG. 1A.

Related limitations may be found in a multitude of independent claims, including claims 18, 21, 30, 32, 38 and 39, as well as claims 19-20, 22-26, 31 and 33-36 that respectively depend therefrom. For example, regarding claim 38 as rejected under § 102 solely over the '944 reference, the reference fails to disclose limitation directed to presenting "an electric field substantially at only one of the first and second junctions." This is also consistent with the Examiner's indication at page 11 of the Office Action, which states that "Mizutani does not teach a gate offset to present an electric field substantially at only one of the two junctions." The '944 reference also does not disclose or even mention an avalanche breakdown (*e.g.*, as in claim 2), which is achievable using such an approach.

Regarding the § 103 rejections, as discussed above, the Office Action appears to be combining secondary references with the "Sin" reference as cited in prior responses of record, and not with the '944 reference as newly-cited herein. Accordingly, Applicant submits that all of the § 103 rejections are improper and should be removed.

While further discussion of the § 103 rejections is believed unnecessary in view of the above, Applicant submits that the Office Action's stated rationale for adding the secondary '696 reference to "have the gate located predominantly over the second region to be more highly integrated as taught by" the '696 reference (as asserted at page 11) has nothing to do with effecting an electric field distribution near a junction, and the rejection has not established that the proposed combination would (or could) operate in such a manner. For example, cited Figure 2 discloses a tunnel transistor in which a gate is located over a heavily-doped degenerative region (N+ region 27), and not over any intrinsic region as claimed. Moreover, the gate 21 is not arranged to cause a field distribution as claimed, and if implemented with the '944 reference, does not appear to be capable of introducing a breakdown condition via channel length adjustment.

Applicant further submits that any modification of the '944 reference to include offset gate structures and/or functions relating to effecting a carrier concentration in an offset portion of an intrinsic region is unmotivated because the '944 reference teaches away from such a modification, and further because such modification would appear to render the '944 reference inoperable for its purpose. Consistent with the recent Supreme Court decision, M.P.E.P. § 2143.01 explains the long-standing principle that a § 103 rejection cannot be maintained when the asserted modification undermines either the operation or the purpose of the

main (AAPA) reference - the rationale being that the prior art teaches away from such a modification. *See KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1742 (2007) ("[W]hen the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious."). *See also In re Gordon*, 733 F.2d 900 (Fed. Cir. 1984) (A §103 rejection cannot be maintained when the asserted modification undermines purpose of the main reference.). In this instance, modifying the gate structure and/or its application of the '944 reference (see FIG. 5A) would undermine its purpose of affecting the potential of an impurity region "as a whole" per the above discussion. In accordance with the aforesaid purpose, the '944 reference thus teaches away from the claimed invention.

In view of the above, all of the §§ 102 and 103 rejections are believed to be improper, and Applicant requests that they be removed.

Notwithstanding the above, Applicant has amended certain claims in a manner that is believed to be consistent with the claims as previously presented and with the above-discussed aspects of the claimed invention. Applicant believes that the amended claims are allowable over the cited references for reasons stated above, and further because the cited references, alone or in combination, fail to teach or suggest claim limitations directed to an offset gate and/or to effecting a change in carriers of an intrinsic region, relative to a first junction and offset from another junction. Moreover, the cited references fail to contemplate or recognize the applicability of such limitations in the context of devices such as those involved in logic or memory for rapid switching applications.

In view of the above, Applicant believes that each of the rejections is overcome, and that the application is in condition for allowance. A favorable response is requested. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is encouraged to contact the undersigned at (651) 686-6633.

Respectfully submitted,

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